## REMARKS

The Examiner is thanked for indicating that claims 3 and 8 would be allowable if written in independent form. Accordingly, applicants present herewith new claims 17 and 18 drawn generally along the lines of claims 3 and 8, combined with the features of claims 1 and 7, respectively, with some changes. Claims 17 and 18 are therefore believed to be patentable in light of the art and allowance is respectfully requested, as well as for dependent claims 19 and 20 from claim 18. Claim 11 is amended. Claims 17-20 are new.

We have reviewed the U.S. Patent No. 6,119,226 to Shiau et al. that has been used by the Examiner for his rejections. The only common feature of the invention with Shiau et al. is that they are in the same technical field, *i.e.*, to memory devices on motherboards to be used to store a system BIOS and other information.

However, it should be noted that Shiau et al. describes how to address a same memory device, of any kind, by using a top-down or a bottom-up method. It does not discuss selecting a memory from a plurality of memories using the claimed technique of this invention.

According to Shiau et al., the above-indicated addressing methods and their corresponding hardware realizations, relate to the possibility of addressing a memory device, indeed. In particular, the bottom-up method starts from BOOT-16K, with row addresses A<17:13>=00000->00001 (in this case, MAIN_128K comprises the row addresses 10000->11111), while the top-down method starts from MAIN_128K addressed by A<17:13>=00000->01111 (in this case, BOOT_16K would be addressed by 11110->11111).

In order to switch from one method to the other, the row addresses A<17:13> (which are devoted to the selection of the different sectors of the considered memory device) are simply inverted. This switching is made by setting (=> top-down) or resetting (bottom-up) the signal issued from the block INVCTL.

On the contrary, the present invention of claims 1-17 specifically relates to a group of memory devices which are pseudo-serial memories each having I/O pins.

In this particular context, the present invention of claims 1-20 relates to the design of an architecture which can select one among different memories, all addressable on a PC motherboard.

Within this invention, due to the presence of different memory devices in a same PC addressing area, a method and a corresponding architecture for selecting only one of these devices is to be provided. In particular, this selection of a memory device can be made according to the top-down or bottom-up methods.

Moreover, it should be noted that, according to this invention, the processor of a motherboard communicates to the different memories through an I/O controller, having the task to communicate with the particular memory which has been addressed among the others.

The memory scheme should thus comprise an architecture having the following features:

a) it should be able to be contacted;

b) it should manage an addressing step which proceeds from the bottom to the top (bottom-up) or from the top to the bottom (top-down) in a memory area wherein other memories (having different capacities) are related, all being addressed according to a same addressing method.

In one embodiment, as claimed in claims 1-17, the memory devices comprise I/O pins of hardware identification having thus the possibility of choosing among a plurality of different memories, such as 8 or 16, in the addressing area of the motherboard. In one example, to which not all claims are limited, an LPC protocol comprises 8 clock cycles during which four bits at once can be transmitted and used to address a memory and since a maximum value of 20 bits is required to address an 8 Mbit memory, in a conventional manner bits from 21 to 31 are used to solve the following two problems:

- find out if the memory is within a top-down or a bottom-up addressing area (bits 25-31);
- locate the addressed memory (bits 21-24).

In other words, generally stated with respect to claims 1 and 7, during the protocol phase wherein the memory address bits are transmitted, first set of bits are compared through a hardware logic by using ID pins. Moreover, other bits are used to discriminate the addressing method (top-down or bottom-up) and enable, through a specifically designed logic, a correct comparison between the first set of bits 21-24 and the ID pins.

More particularly, the specifically designed logic allows a direct comparison of the address bits with the ID pins in case of a bottom-up addressing method, and an inverted comparison in case of a top-down addressing method.

The above-described logic, which automatically decodes the addresses A<31:21>, is enabled by a CAM.

In summary, we would emphasize that Shiau et al. relates to a fully different problem with respect to the present invention, *i.e.*, how to correctly address different sectors of a memory device, in case of a top-down or a bottom-up addressing method.

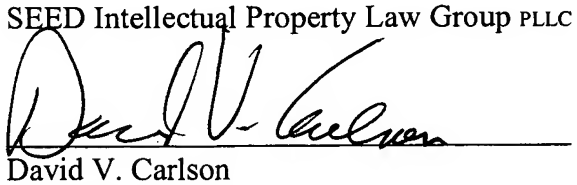
While such a problem is also solved within the present invention of a memory architecture, the proposed solution is patentable as being able to select one memory in some embodiments and one memory device in other embodiments from a group and also perform specific addressing to that selected device.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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